Cl 2 Cont'd.

a control module for programming the first, second and third data buses, and the error check module to operate according to the [a] plurality of error processing modes, wherein data transferred from the edit buffer to the first data port is checked for errors and an error check work is generated for data transferred from the first data port to the edit buffer.

## REMARKS

*Information Disclosure Statement*

The Examiner stated that Applicant's information disclosure statement filed 7/22/97 failed to comply with 37 C.F.R. § 1.98(a)(2) because copies of the references were not included. Applicant respectfully draws the Examiner's attention to the fact that the present application is a divisional application filed under 37 C.F.R. § 1.60, as stated in the transmittal sheet filed with the present application. The references listed on the 1449 form were submitted in the parent case, serial number 08/474,397, now U.S. Patent number 5,854,800 on Jun 7, 1997, and that fact was stated in the IDS transmittal. Also in the IDS transmittal was the statement that Applicant filed the IDS in accordance with 37 C.F.R. § 1.98(d) so that copies of references previously cited by or submitted to the U.S. Patent Office in conjunction with a prior, related case were not required. Therefore, Applicant respectfully requests that a copy of the 1449 form, marked as being considered and initialed by the Examiner, be returned with the next official communication.

*Amendments*

Applicant has amended independent claims 8, 14 and 15 to more clearly point out Applicant's invention, in particular the support for multiple data protocols, the programmable edit buffer, and the operation of the multiple buses in providing for bidirectional data flow through the system [Specification: page 3, line 22 through page 8, line 2]. The operations and data flow through Applicant's system is summarized below with reference to Figure 1 of the present application to illustrate these unique features.

Data which is to have an error correction word generated is presented at the first port (IOD), stored into an input buffer (120) and latched into a data latch (110) for input into an error word generator (130). The error word generated from the data is transmitted on a third bus (bus comprising lines controlled by gates 181 and 182) for storage in an edit buffer (160). The data is

also transferred on a first bus (105) to the edit buffer. The contents of the edit buffer are then available through a second port (the combination of C[0:7], HE[0:31], PP[0:31]). Thus, data flows from left to right through the system illustrated in Figure 1 when generating an error word for data input at the first port.

Data having an error correction word and which is to be checked for errors is input into the edit buffer through the second port (bus comprising lines controlled by gates 187, 188 and 189). The data is transferred through data outputs controlled by gates 183, 185 onto the first bus to the error word generator and through data outputs controlled by gates 184, 186 onto a second bus (106) to an output latch (140). A compare circuit (170) checks the error word generated from the data against the error correction word stored in the edit buffer and transmitted. If the compare circuit signals that the data is error-free, the data is transferred from the output latch to the first port; optionally, if the data is in error, it can be corrected before being transferred to the first port. Thus, data flows from right to left through the system illustrated in Figure 1 when checking data input from the second port for errors.

Because of the unique structure of the invention, data flows in opposite directions through the system depending on whether an error word is to be generated from input data or whether input data is to be checked for errors. Because the buses operate in parallel, data can flow in both directions simultaneously. Furthermore, because the format of the edit buffer is programmable, the invention is readily adaptable to use with multiple data protocols, such as having raw data in all the edit buffer, raw data in a portion of the edit buffer and header data in another portion, or header data in one portion and prepend/postpend data in another.

*Rejections Under 35 U.S.C.§ 102*

Claims 15-24 are rejected under 35 U.S.C.§ 102(e) as being anticipated by Zook et al. (U.S. Patent No. 5,602,857). Applicant does not admit that the Zook patent is prior art but believes the present invention is distinguishable from Zook for the reasons cited below. Nonetheless, Applicant reserves the right to swear behind the Zook reference at a later time by filing an affidavit under 37 C.F.R. 1.131 showing a completion of the invention prior to October 18, 1994.

Applicant respectfully submits that Zook does not disclose all the features of their invention as claimed in independent claim 15, and claims 16-24 which depend upon claim 15. As explained above, claim 15 claims a bidirectional system in which different operations are performed on the data depending on the direction the data is flowing through the system. Zook, on the other hand, simply generates a CRC word for data placed in a buffer by a host computer so that when the data is stored to media, it can be checked for errors prior to being written. The exact same operations are performed when the data is read into the buffer from the storage media, prior to being sent to the host. [Zook: column 2, line 57 through column 3, line 17].

Furthermore, Applicant also respectfully disagrees with the Examiner that the bus structure of Zook's system anticipates the bus structure of Applicants' invention. Zook does not disclose the arrangement and functions of the elements of Applicant's invention in enabling data flow through an error correction circuit as claimed in amended claim 15. Because the buses and other components are interconnected differently in Zook, the resulting data flow through Zook's system is also different. Applicant respectfully reminds the Examiner that a reference cannot anticipate a claim unless the *identical* invention is disclosed [M.P.E.P. §2131]. The mere fact that Zook discloses a series of interconnected buses and subsystems to perform error correction is insufficient to anticipate Applicant's invention unless those buses and subsystems are arranged and function as claimed by Applicant..

Finally, Applicant respectfully submits that the Examiner has not pointed out the elements of Zook's bus structure that render it capable of supporting the bidirectional, programmable data flow of Applicant's invention. The Examiner has merely stated that the parallel and programmable features of Applicant's buses are *inherent* in Zook's bus structure. Applicant has studied Zook and can find no disclosure that Zook's buses operate in parallel as claimed in claim 15. In addition, Zook's error correction system operates in a single mode and Zook does not disclose the capability of programming his invention to handle different data protocols as is disclosed and claimed by Applicant.

Zook discloses only three user-supplied parameters related to buffer 1100: the type of memory used for buffer 1100, whether to append the error correction word (CRC) to the hard disk sectors stored in buffer 1100 (register APPEND BUFFER CRC), and the number of bytes to generate for the CRC (register # BUFFER CRC BYTES) [Zook: col. 8, lines 8-14]. Registers

APPEND BUFFER CRC and # BUFFER CRC BYTES determine how CRC words are applied to the hard disk sectors transiting Zook's system but have no effect on the configuration of the buffer 1100 itself. Additionally it should be noted that Zook's invention works with sectors of data and has no knowledge of the protocol of the data stored within a sector. In contrast, Applicant's edit buffer itself is programmatically configurable to handle multiple protocols of the data stored therein. Applicant respectfully reminds the Examiner that she must provide rationale or evidence tending to show inherency in a reference [M.P.E.P. § 2122] when the reference is silent with regard to elements claimed in the application.

With regard to claims 16-18, as argued above, Zook does not teach programming multiple buses to function as claimed by Applicant.

With regard to claims 19-20 and 22, Applicant respectfully points out that the Examiner has not cited any disclosure in Zook that anticipates an edit buffer with a data portion for storing a data word comprising either a header portion and a raw word portion, or a header portion and prepend/postpend data portions. Although Zook discusses a header (ID) subsection, the header (ID) subsection performs error correction on a sector ID, not on the header portion of a data word stored in a programmable edit buffer. A hard disk sector ID, as well-known in the computer art, is not a part of the data words stored in the sector, but identifies a physical location on the disk for the entire sector and is maintained in a table separate from the data on the disk.

With regard to claims 21 and 24, the Examiner stated that Zook does not disclose the function but that the feature is "well with in the scope of the invention as taught by Zook." Applicant respectfully traverses such an assertion since the invention disclosed in Zook is not the same as that claimed by Applicant and thus, Zook does not have a scope commensurate with claims 21 and 24.

Because Zook does not teach the arrangement and function of the elements of Applicant's invention as claimed in amended claim 15, Zook cannot anticipate claim 15, or claims 16-24 which depend from claim 15. Therefore, Applicant respectfully requests the withdrawal of the 35 U.S.C. 102(e) rejection of claims 15-24 over Zook.

*Rejections Under 35 U.S.C.§103*

Claims 8, 11-14 are rejected under 35 U.S.C.§103(a) as being unpatentable over Zook et al., in view of Peterson et al. (U.S. Patent No. 5,241,546). Applicant respectfully traverses the rejections because the Examiner has failed to state a *prima facie* case of obviousness.

The Examiner has relied on Peterson to teach the latch element and function of Applicant's invention as claimed in claims 8 and 14, and claims 11-13 which depend from claim 8. Paterson does not teach a bidirectional, programmable error correction system which operates in a plurality of error processing modes, as claimed by Applicant. Because neither Zook nor Paterson disclose such a system, the combination of them cannot render Applicant's invention as claimed in claims 8 and 11-14. Therefore, Applicant respectfully requests the withdrawal of the rejection of claims 8 and 11-14 under 35 U.S.C. 103(a) over the combination of Zook and Paterson.

CONCLUSION

Applicants believe the claims are in condition for allowance and request reconsideration of the application and allowance of the claims. The Examiner is invited to telephone the below-signed attorney at 612-373-6904 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **February 16, 1999**.

Name Daniel J. Kluth / Signature Daniel J. Kluth